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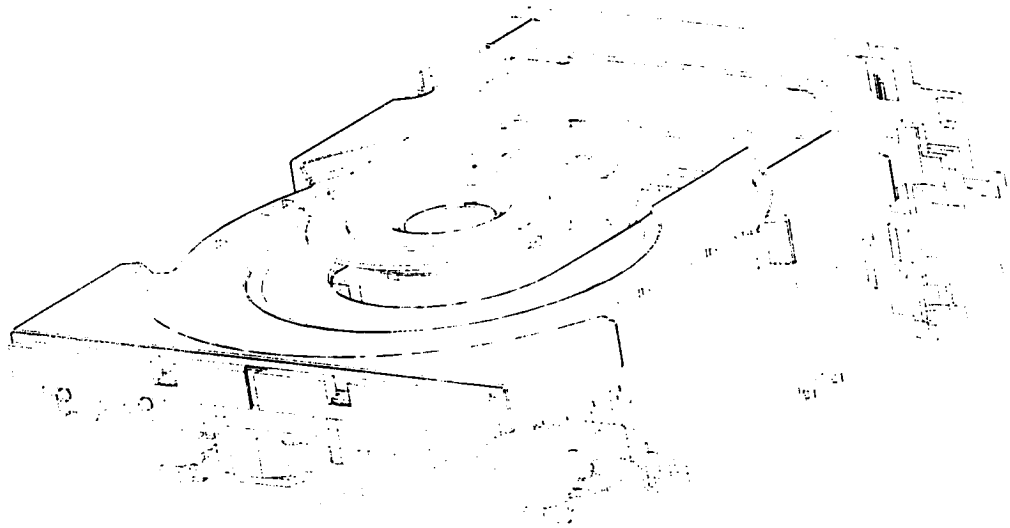
ECO-SL MKIII CD MODULE

Specification, Version 2.2



COMPACT disc DIGITAL AUDIO

COMPACT disc DIGITAL AUDIO TEXT

COMPACT disc Recordable ReWritable PLAYBACK ONLY

Subscr

PHILIPS

CHN:			PERFORMANCE SPECIFICATION		
	1	Module ECO-SL MK3 CC	3103 308 51930		98-02-13
97-10-15	2				98-01-22
98-02-13	3				
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1. General

ECO-SL MKIII is a self-contained CD Module derived from ECO-SL MKII with additional features as

- CD-R/W playback of finalized discs possible
- CD-TEXT decoding
- I^2S Interface for connecting external DAC
- both coaxial and optical digital out break away PCB part of module.

It is succeeding ECO-SL MKII and hardware and software wise fully backwards compatible to it.
The module includes following functions :

- · CD Mechanism
- · CD Tray Loader Mechanism
- · CD Electronics (HF Preamplifier, CD Servo & Decoder, DAC, tray driver)

The CD Electronics can be used with CD Mechanism, but without Tray Loader Mechanism; this setup is called the "flap version" of ECO-SL MKIII. The design of the flap loading mechanism is set-related and thus not treated in this specification. See MC170 for reference.

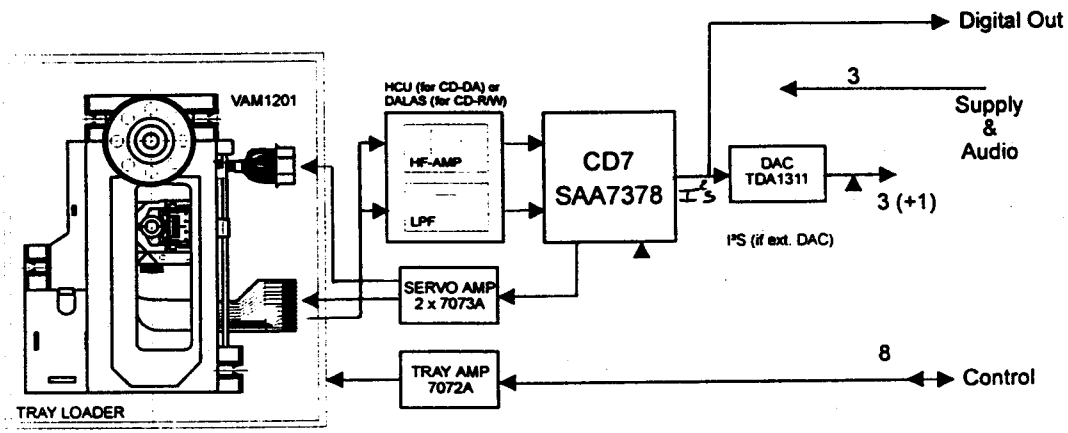
NOT included are:

- · Control function (microprocessor): has to be handled by external (set)-microprocessor
- · Ornamental CD Tray cover: styling and set-related
- · Cable for connecting optical or coaxial out break-away PCB to main module

2. Key Components

· CD Mechanism :	VAM1201
· CD Loader :	Mechanical part of CD-SL (3103 308 51170) or new HK tool (3103 309 04770)
· HF-Amplifier:	DALAS TDA1302 + HCU04 (R/W-Versions) or HCU04
· CD Decoder/Servo:	SAA7378 (low cost CD7)

Block Diagram:

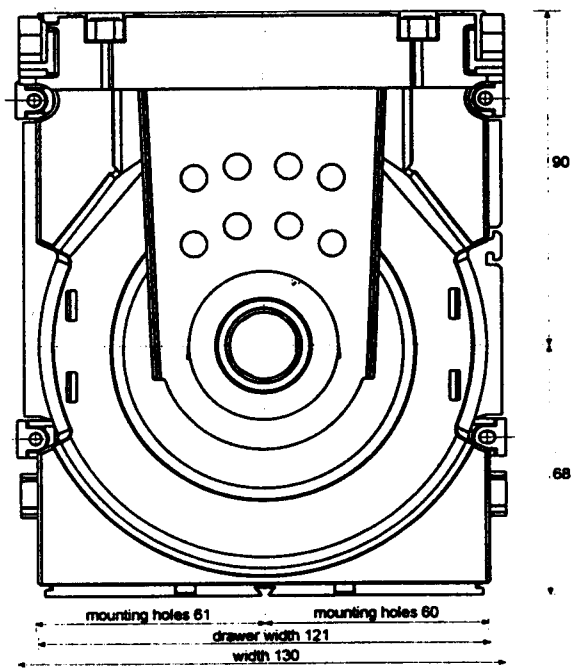


5. Interfaces

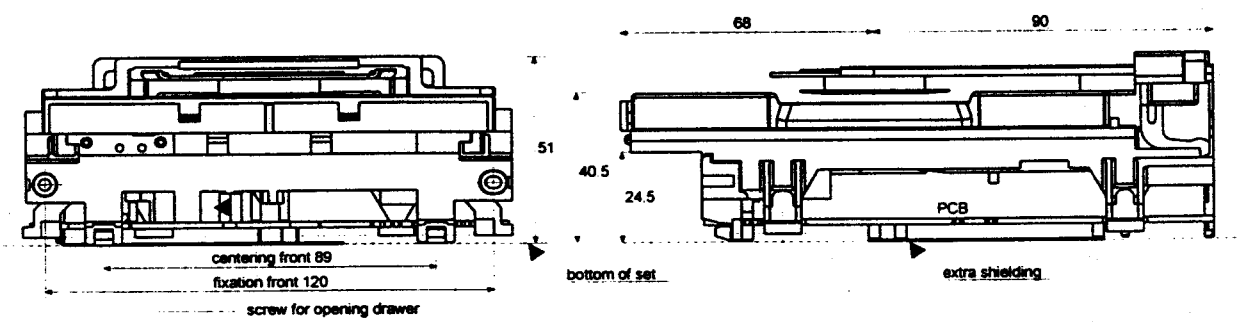
5.1 Mechanical

Tray loading mechanism: dimensions same as CD-SL, see CD-SL, sheet 112-01 (Shortloader 1 Assy, 3103 308 5117).
Flap loading mechanism: mechanical part of flap loader not part of module. See MC170 for reference.

- Emergency opening screw can be accessed from the bottom of loader



travel stroke drawer: 131.5



5.2 Electrical

Interface connections used for all applications of ECO - SL MKIII:

5.2.1 Supply and Audio Interface

Conn. 1802, 6 (7) pol JST EH horizontal, linked to combi board of set

1802

▫	6 (7)	+A	servo supply voltage, 6 - 13.5V, see chapters 7, 10.4	
▫	5 (6)	GND	servo and dig. ground	
▫	4 (5)	+5	5V switchable for digital IC's, ±5%	
▫	3 (4)	ANA-R / IIS_WS	analogue output right /	I^2S Word Select
▫	2 (3)	AGND / IIS_BCK	analogue ground /	I^2S Bit Clock
▫	1 (2)	ANA-L / IIS_SDA	analogue output left /	I^2S Serial Data
▫	- (1)	KILL	inverted kill signal (opt.)	CD7 kill signal [1]

ad 1): for IIS interface, KILL output of CD7 is connected directly to pin7 of 1802.

5.2.2 Control Interface

Conn. 1804, 8 (6) pol JST EH horizontal, linked to control (front) PCB of set

1804

▫	8	(6)	SICL	I	Clock line for CD7
▫	7	(5)	GND	-	GND, connected to pin2 of 1802, for EMC improvement
▫	6	(4)	SILD	I	Latch line for CD7
▫	5	(3)	DATA	I/O	bidirectional data line for CD7
▫	4	(2)	RESET	I	Reset for CD7 (active low)
▫	3	(1)	TRAY_SW	O	tray switch (refered to GND). No internal pull up.
▫	2	-	TRAY+	I	tray out if low (tray version only)
▫	1	-	TRAY-	I	tray in if low (tray version only)

Tray in/out controlled with 2 lines (TRAY+, TRAY-). For flap version, conn. 1804 is 6p, "TRAY_SW" indicates the position of leaf switch.

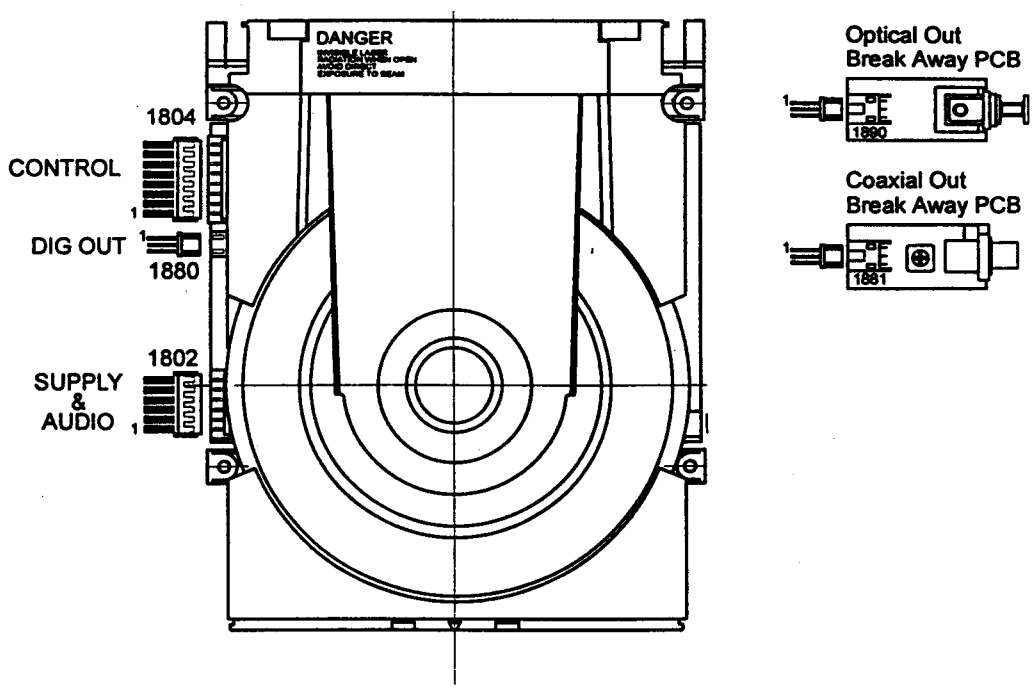
Interface Connections used for special applications:

5.2.3 Digital Out

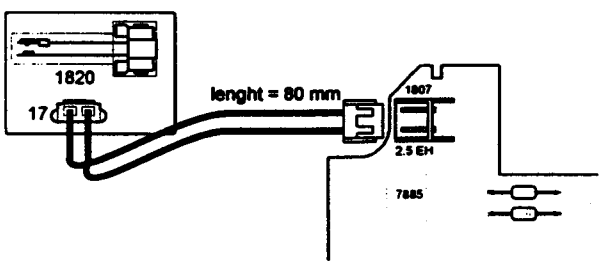
Conn. 1880, Digital Out, 3p JST PH 2.0 horizontal
Explanation see 10.7.

1880

		Coaxial Out	Optical Out
▫	1	EBU-GND	EBU-GND
▫	2	DOBM	DOBM (TTL)
▫	3	SHIELD	+5V



5.2.4 Leaf Switch Connector (flap version only)
Conn. 1807, 2p JST EH horizontal



5.2.6 Correction Flag (CFLG) Output

Conn. 1850, 2p JST PH horizontal
This output can be used for measuring the BLER (Block Error Rate) of the CD Decoder by means of an appropriate measuring equipment. Output needs an external 10k pull up to +5V.

1850

▫	1	GND	-
▫	2	CFLG	O

6. Environment Conditions

Temperature: operating : -10 °C - 65 °C for +A= 6...12V (except VAM1201)
-10 °C - 55 °C for +A= 6...13.5V (except VAM1201)
storage : -25 °C - 70 °C (except VAM1201)
(VAM1201: see spec. 5.1, 17.02.95: operational temperature range: 5 - 55°C)

Climate : all climates acc. UAN-D1590

Shock : For specified shock performance, +A must be between +8 and 13.5V,
a +A=6...8V leads to degradation of shock performance.
operating : ±X direction (3ms) ≥5 g (ECO-SL MKIII in AZ1518 Z33)
±Y direction (3ms) ≥5 g (")
±Z direction (3ms) ≥3 g (")

7. Safety

IEC 65/UL1492
Compliance to safety requirements at module level is defined at following supply conditions :
+A (Conn. 1802) : 12V/Imax = 2.5A
Maximum voltage at +A supply: 16V (elcaps withstand 25V)
Maximum current when +A is connected to GND: I_{max}= 2.5A

Minimum required current when at minimum +A (6V): I_{min}= 1.25A (PTC protects TDA7073A)
Minimum required current when at minimum +A (8V): I_{min}= 1.00A (NFR protects TDA7073A)

Please note that for full supply voltage range of +A (i.e. 6 ... 13.5V), item 3847 (PTC) has to be stuffed , for supply voltage range +A = 8 ... 13.5V, item 3847 can be replaced by item 3841 (NFR).

+5 (Conn. 1802) : 5V/I_{max}= 1.25A
Maximum voltage at +5: 6.3V
All elcaps are at least 16V types, except item 2866, which is 100µ/10V (for internal DAC only).

For deviating supply conditions the safety requirements have to be re-evaluated by the applicant.

9. Quality

AQL : 0.4 maj.
0.65 min.
Field Quality: ≤ 650h: < 1% customer returns (with a VAM1201 of 0.4%)
≤ 3300h: < 3% customer returns

10. Technical Data

If not specified otherwise : PQR for Portables and MMM, Class II

10.1 Audio Performance

10.1.2 I^2S Interface (External DAC)

For a superior audio performance, an external DAC has to be used in combination with the I^2S Interface of ECO-SL MKIII. Layout cells for TDA1545 (CC) and TDA1549 (BCC) can be found in sheet 185 of TPD. Be aware that the I^2S lines carry HF signals and keep the cable as short as possible. Various I^2S, EIAJ and SONY DAC formats, both baseband and 4 times oversampled, can be selected via software setting of CD7. There's no master clock available for external DAC.

The performance of the external DAC's can be influenced by the rise/fall times of the IIS-signals, dependent on the D/A-type. Bitstream or BCC DAC's generally require sharp edges of the bitclock BCLK.

- TDA1545 accepts TTL levels
- TDA1549 needs 30/70% CMOS levels, depending on the DAC's supply voltage

- Series resistors at the receiving end should not be higher than 100R
- do not use capacitors at receiving end
- Maximum allowed cable length depending on EMC/DAC performance

IIS Logic Levels:

Version	CC		BCC	
Signal	Vhigh	Vlow	Vhigh	Vlow
IIS_WS	3.3V	0.3V	4.0V	0.5V
IIS_BCLK	3.3V	0.3V	4.0V	0.5V
IIS_DATA	3.3V	0.3V	4.0V	0.5V

10.2 Playability

satisfies XUW0010-EN, 1995-03-02, p.112, chapter 25.3

For CD-R/W, no PQR requirement is established yet. ECO-SL MKIII plays following R/W-Test CD's:

- CD-R/W Low Reflection Audio Disc 7104 099 96581: all tracks
- CD-R/W High Reflection Audio Disc 7104 099 96601: all tracks
- CD-R/W Printed Audio Disc (double 444A printing) 7104 099 96611: 600µ black dot, fingerprint

Jitter: for Testdisc 444A: 15ns typ., for R/W Testdisc with double 444A printing: 20ns typ.

10.4 Supply Voltage Range & Current Consumption

Supply Voltage: +5: -5/+10%. (5.6V -0.5/+0.4V as version for Z33)
+A: 6...13.5V nominal 10V (item 3847 PTC stuffed)
+A: 8...13.5V nominal 10V (item 3841 NFR stuffed instead of 3847)

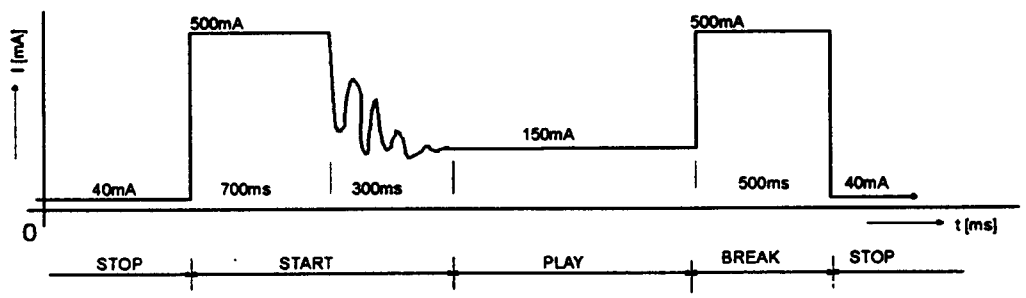
Restrictions: - for +A≤8V decreased shock performance.
- for +A≥12V temperature range -10..55°C

Attention: after power on of +5 voltage, it will take max. 1.5sec until supply voltage of internal DAC is settled. Before, CD7 decoder is not allowed to send I²S data to the DAC in order to avoid latch up.

Current Consumption:

Mode	+5V	+A (12V)
Stop	40 mA_{typ}	45mA_{typ}
Play	100mA_{typ}	150mA_{typ}
Start Up	100mA	500mA_{max}

For laser diode at end of lifetime, add 30mA to +5V supply current.
Next figure shows typical current on +A line:



Maximum ripple:+5V: ripple determines audio performance of internal DAC. Measurement shows a SNR dependency of ≈0.3dB/$mV_{rmsripple}$ (100Hz ripple on +5 line)
Line drops: +A: 1.5V_{pp} with max. slope of 50 mV/s

10.5 Mechanical Noise

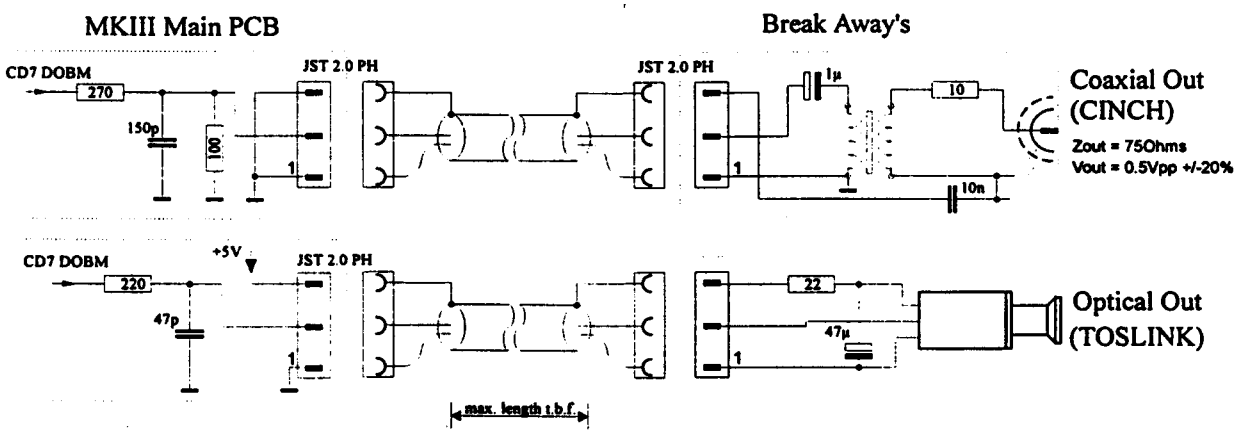
Measured in Z7 AZ2705 with Brüel & Kjaer Sound Level Meter 2230 according UAN- L1059, Part II, 2.8.2

Direction/ Noise (dB_A)	Front (10cm)	top (10cm)	left (10cm)	right (10cm)
PLAY	32	32	26	27
CUE/REVIEW	34.5			
PAUSE				
Track Access	34			
Tray Open/Close	64.6			

10.6 Tray Open/Close Time

1.7s ± 0.5s. Tray can be opened and closed even when +5V supply switched-off. Tray speed slightly depends on value of +A voltage and external series resistors in TRAY+, TRAY- control lines. EMC series resistors in those lines on front board should not exceed 2.2kΩ.

10.7 Digital Out



Digital out can be realized as either coaxial- or optical-output. For reaching the required accuracy of the clock signal, the ceramic resonator is replaced by a crystal.

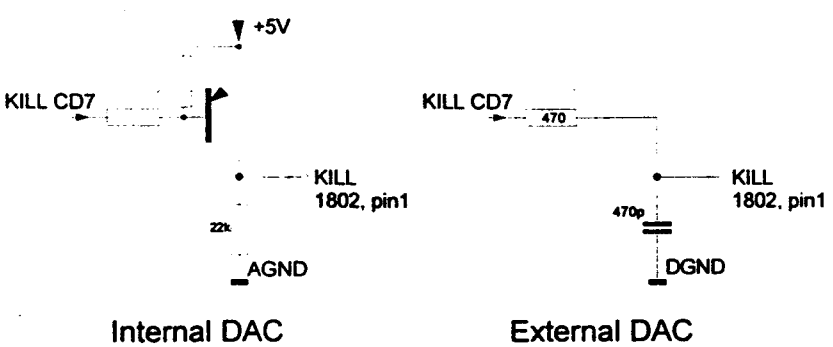
- Coaxial Out: all components except cable between main and break away PCB are part of MKIII. Output format is according IEC958 (see there).
- Optical Out: Transmitter located at break-away PCB. Shielded 3p cable additionally needed. Output signal at pin 2 of con. 1880 provides TTL levels (H≥2.4V, L≤0.8V). **Please note that Optical Out without additional electronics cannot be used in versions with CD-R/W compatibility due to interference of the high speed DOBM signal to the HF front end. See CD753 for alternative solution.**
- Digital Out present: can be read by the µC via versatile input V1 (CD7, pin 62). "L" = dig. out present, "H" = no dig. out present
- It should be noted that the CD7 audio level /mute command will also effect digital out.

10.8 Correction Flag (CFLG) Output

This output can be used for measuring the Block Error Rate of the module. For signal timing, see specification CD7.

10.9 KILL-Output

for internal DAC version, optional, KILL active high, else low (22k to AGND)
for I²S version: KILL active low, only RC filtered



10.10 Miscellaneous

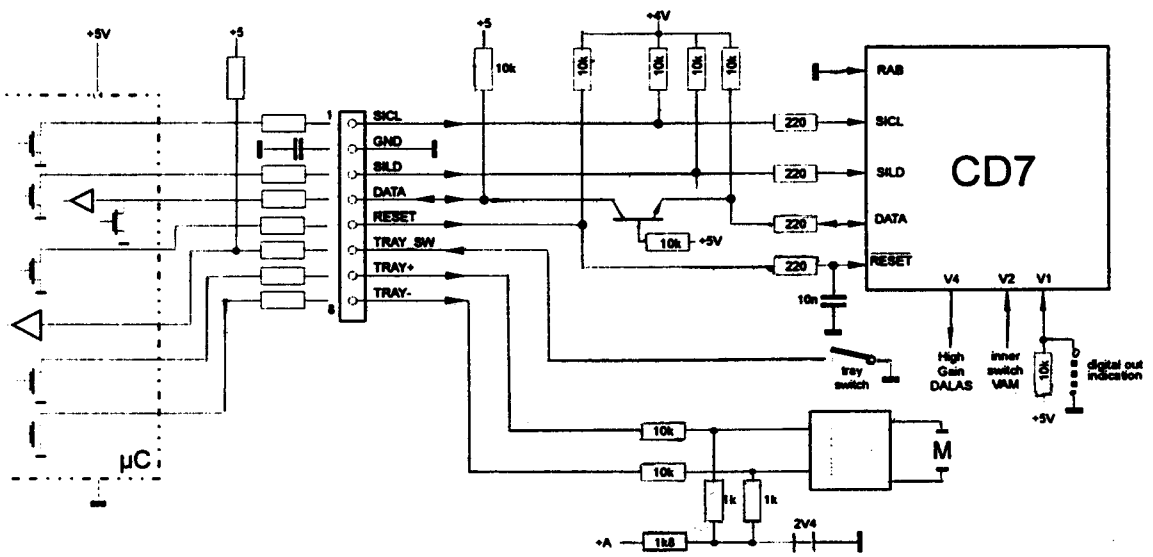
- Inner Switch of VAM1201 mechanism is read in on versatile pin V2, pin 63 of CD7.
- Spindle motor is controlled in PWM mode (2 line mode)

11. Control Interface

The control interface can be splitted in an interface for controling the CD-LSI CD7 (pin1 - pin 5) and the tray control interface (pin 6 - pin 8). Both parts of the interface are independent from each other, tray control (i.e. moving tray in or out) is possible as long as +A is connected to the ECO-SL.

As 3 of the 4 CD control lines are inputs to the ECO-SL (SICL, SILD, RESET), some effort is needed only to convert the logical levels for the bidirectional DATA line.

The next picture shows a block diagram of the Controller Interface:



11.1 Input Signals

All input signals should be used in combination with open drain µC ports. For SICL, SILD and RESET pull up resistors are incorporated on the module. For voltage levels see 11.4.

SICL	*Clock* CD7, input to CD7. 10kΩ internal pull up. For timing refer to data sheet for CD7.
SILD	*Latch Data* for CD7, input to CD7, timing see CD7. Internal pull up (10kΩ)
RESET	Reset input for CD7, active "L". Internal pull up (10kΩ), 10nF to GND. This line has to be tied to "L" immediately after power up to avoid lens knocking. µC can start communication with CD7 1ms after RESET line went from low to high.
TRAY+, TRAY-	- Level: "L" ≤ 0.25V, "H" = high Z of set µC - for both TRAY+, TRAY- open drain µC outputs are mandatory - no external pull up allowed - max. differential voltage between TRAY+ and TRAY- in tray stop mode in order to avoid too high bias voltage across tray motor: ±0.2V

- input resistance 33kΩ. Please note that an additional series resistor in this line will lower tray speed; this effect will be neglectible for series resistors ≤ 2.2 kΩ.

TRAY+	TRAY-	Tray
L	L	(stop) 1)
H	L	moves in
L	H	moves out
H	H	stop, standby

1) not allowed, trough tolerances of µC open drain output transistors, a bias across tray motor may occur. For tray = stop, both open drain ports of the µC should be switched to logical 1.
Remark: Basically, tray control can be done by means of the TRAY+ control line only. In this case, a 3-state board is needed for controlling TRAY+, TRAY- is not used. In this case, connector can be reduced by 1 pin.

TRAY+	TRAY-	Tray
L	n.c.	moves out
high-Z	n.c.	stop
H	n.c.	moves in

11.2 Bidirectional Signals

DATA *Data* signal for CD7. Bidirectional line, internal 10kΩ pull up to +5V.
For timing see CD7.

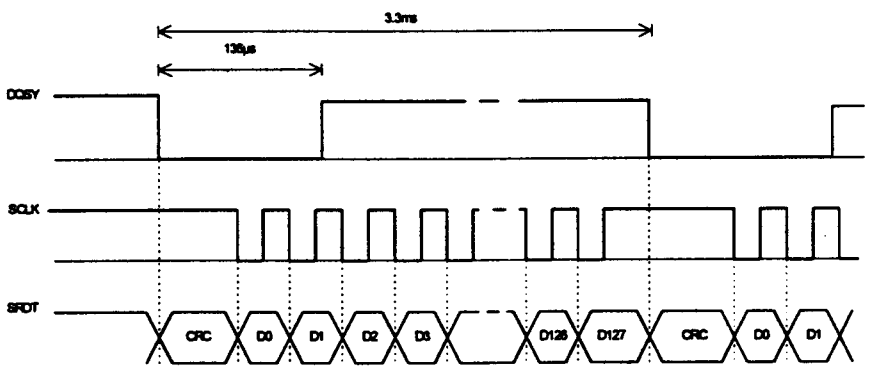
11.3 Output Signals

TRAY_SW mechanical switch for Tray Loader, GND if tray in outmost or inmost position, else floating. External pull up required.

11.4 Signal Levels

Logic Levels:	Inputs:		SICL, SILD:	"L"≤ 1.0V, "H"≥ 2.8V
			RESET:	"L"≤ 0.7V, "H"≥ 3.5V
			TRAY+, TRAY-:	"L"≤ 0.25V, "H"= high Z, Rin = 33kΩ
	Bidir:	Input:	DATA:	"L"≤ 1.5V, "H"≥ 3.5V
		Output:	DATA:	"L"≤ 1V, "H"≥ 4V
	Output:		TRAY_SW:	GND if active, else floating

The timing requirements for the communication between CD-Text IC and µController are as shown below: During TOC-reading, the set-µC has to serve an interrupt every 3.3ms. Within this interrupt, 128 data bits have to be read by the µC. When using Toshiba µC TMP87XX70, it's recommended to use Ports P3.2 and P3.3 (serial clock and serial input) for aquiring CD-Text data.



Signal DQSY is used as an interrupt input signal for the microcontroller. After the falling edge of DQSY the microcontroller sends the clock signal 'SCLK' . The serial data is then read synchronously to this clock signal into the microcontroller.

- Output Levels: DQSY, SRDT: Vlow<0.5V, Vhigh>3.8V; push pull output.
- Input Level: uP_CLK: Vlow<0.5V, internal pull up resistor, use open drain at µC.

13. Application Notes

13.1 Supply / Supply switching Concept :

There are 2 supply inputs to the module :

+A Conn. 1802 (Supply)
This voltage supplies servo driver amp's etc. and can be applied continuously; there is however a current flow of $40mA_{typ}$ (bias current of servo driver amp's, etc.) even if the 5V Supply (see below) is switched off. A zero power standby solution can be realized by switching +A line off externally.

+5 Conn. 1802 (Supply)

This voltage supplies the digital circuit (Servo Processor, Decoder, DAC) and shall be applied only if the CD part has to be active (e.g. mode selector in position CD) to prevent interference to other parts of the set (tuner) in non-CD modes.
The 5V line is also used to supply the DAC; for a good audio performance care has to be taken to keep the low frequency ripple as low as possible.

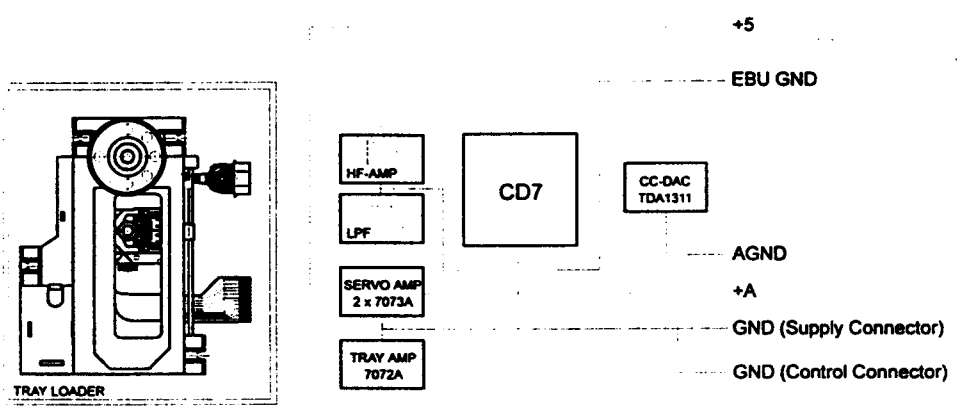
13.2 Ground Concept

GND Conn. 1802 (Supply) 'Supply Ground'
This is the ground connection to servo amplifiers, digital circuits. etc.
As this line carries high and 'noisy'currents it shall be connected directly to the central ground reference point of the set (main filter capacitor in the power supply)

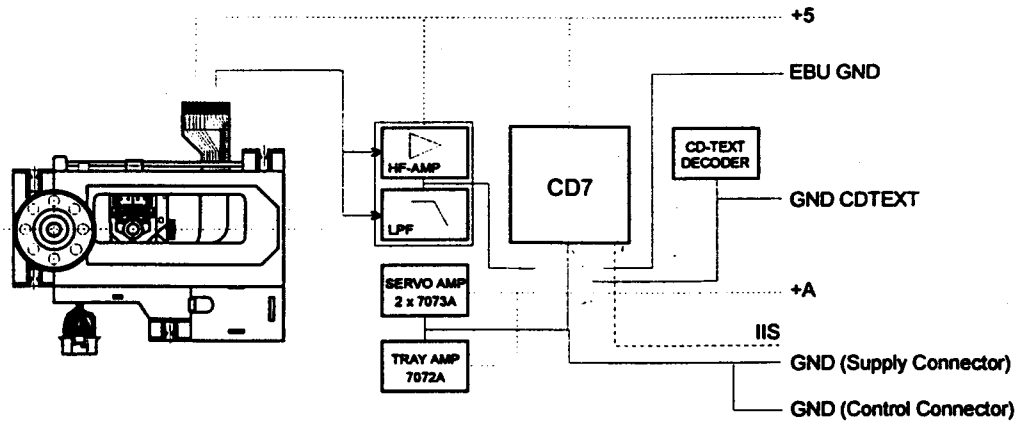
AGND Conn. 1802 (Audio) 'Audio Ground' (for internal DAC version only)
This is the ground connection for the audio output part (DAC TDA1311) and shall be routed in parallel to the audio signals. Ultimately it has to be connected to the same potential as the supply ground. GND and AGND are *not* connected inside the ECO-SL module.

GND Conn 1804 (Control) 'Digital Ground'
Same ground as 1802, GND. Should be used to improve EMC. Please note that this line is only allowed to carry signal return currents.

The next figure shows supply and grounding concept of ECO-SL MKIII with CC DAC.



The next figure shows supply and grounding concept of ECO-SL MKIII with IIS-Interface



14. Compatibility ECO-SL MKIII to ECO-SL MKII

Changing over from ECO-SLMKII to ECO-SL MKIII:
- control interface: replace 9p connector on front by 8p connector, line 9 of MKII (GND) was deleted for MKIII
- some evaluations, e.g. passive/active radiation, ESD, etc. have to be done again
- MKII software can be reused, software adaptions necessary when playing CD-R/W
- MKIII modules with R/W-compatibility require a new software. As the CD-R/W-system is far more sensitive to external influences than the standard version, special attention is needed with regard to EMC, ESD, etc.

Control Interface:

#	ECO-SL MKII		#	ECO-SL MKIII
1	GND	≠		not existing
2	SICL	=	1	SICL
3	GND	=	2	GND
4	SILD	=	3	SILD
5	DATA	=	4	DATA
6	RESET	=	5	RESET
7	TRAY_SW (door switch)	=	6	TRAY_SW (door switch)
8	TRAY+ (not for flap version)	=	7	TRAY+ (not for flap version)
9	TRAY- (not for flap version)	=	8	TRAY- (not for flap verision)

The only difference in the control interface is the missing GND line at the control interface.